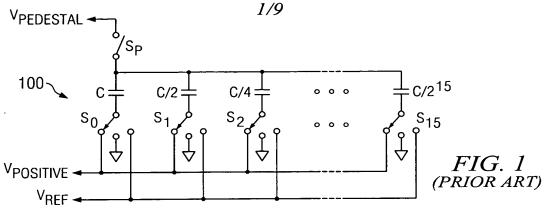
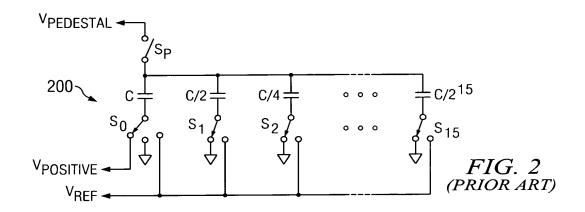
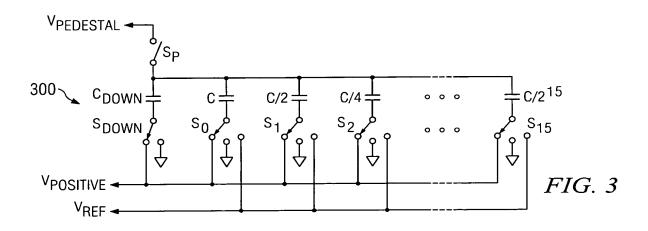
Inventor: Docket No.: Attorney:

TI-35905

Phone: 602-382-6250 Express Mail: EV325938879US







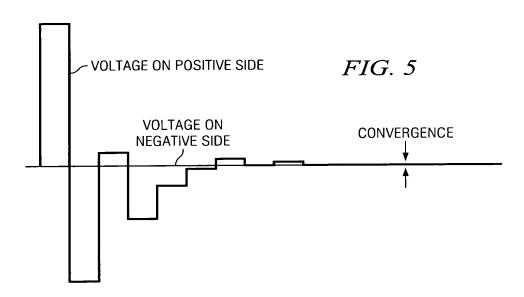
$$V_{PEDESTAL}$$
 $\stackrel{S_{P}}{\longrightarrow}$ $\stackrel{2C}{\longrightarrow}$ $\overrightarrow{\nabla}$ $FIG. 4A$

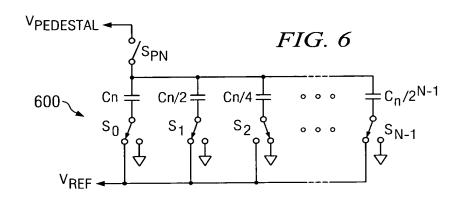
VPEDESTAL
$$402 \checkmark S_P$$
 $2C \checkmark FIG. 4B$

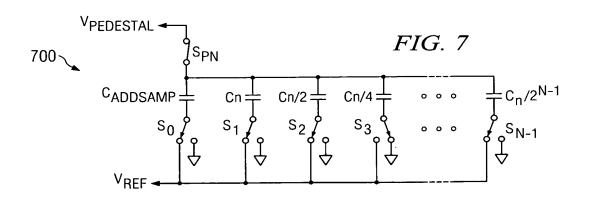
Inventor: Robert E. Seymou
Docket No.: 38880.7200
Attorney: R. Lee Fraley
Phone: 602-382-6250
Express Mail: EV325938879US

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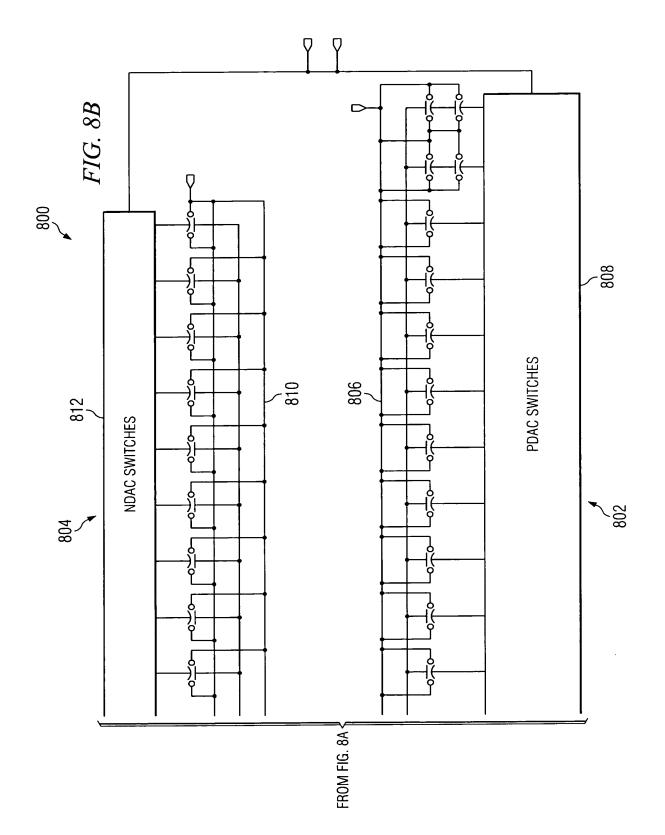
Title: M&C for Gain and/or Offset Correction in a Capacitor Digital-to-Analog Converter Inventor: Robert E. Seymour Docket No.: 38880.7200
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3/9 TO FIG. 8B C/32 808 810 806 812 C/16 NDAC SWITCHES PDAC SWITCHES C/8 -814 PEDESTAL SWITCH CIRCUIT C/4 **C/**5 VPEDESTAL C> 802 V_{NEGATIVE} □ VPOSITIVE □ 818 **SWITCH FOR SWITCH FOR** VSIGNAL VREF LOGIC BOOTSTRAP FIG. 8A 820

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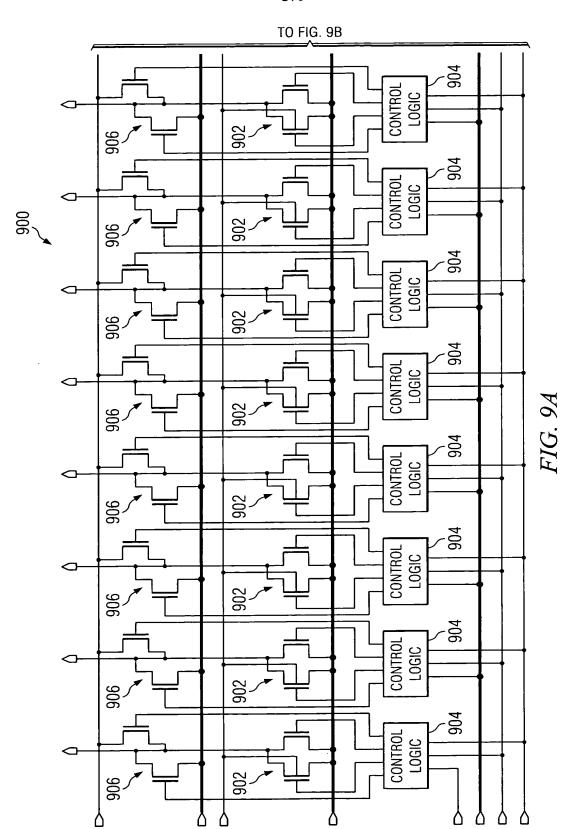




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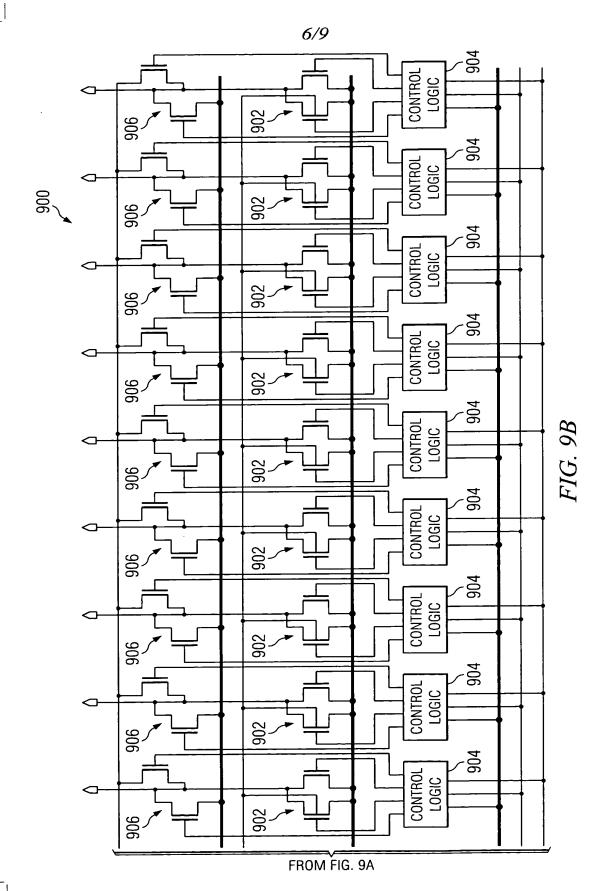
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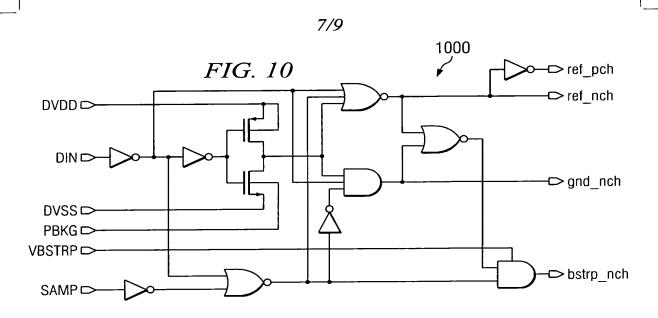
Title: M&C for Gain and/or Offset Correction in a Capacitor Digital-to-Analog Converter or: Robert E. Seymour t No.: 38880.7200

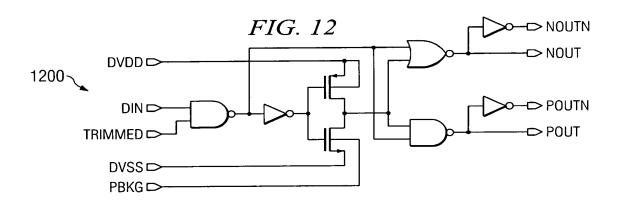
Inventor: Docket No.: Attorney: Phone:

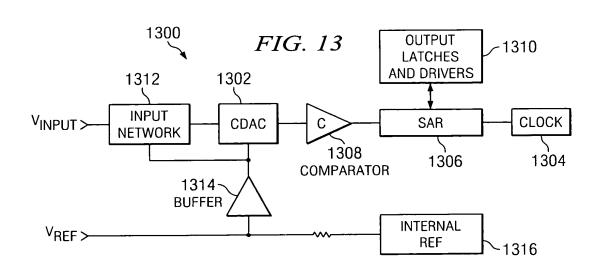
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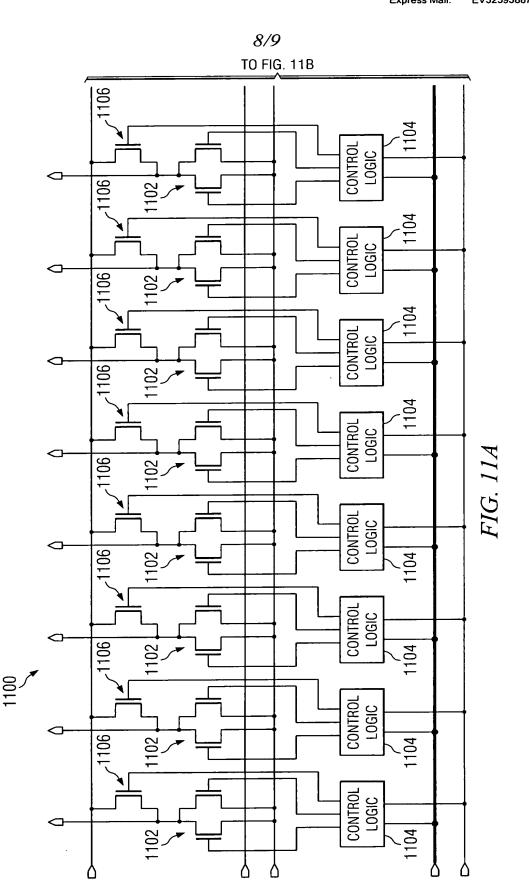






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